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Fast Charge Pump Circuit for PLL using 50nm CMOS Technology

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Abstract: PLL being a mixed signal circuit involves design challenge at high frequency. This work analyses the design of a mixed signal phase locked loop for faster phase and frequency locking. The performance of charge pumps depends heavily on the ability to efficiently generate high voltages on-chip while meeting stringent power and area requirements. The paper presents a High Speed CMOS charge pump circuit for PLL applications using 50nm CMOS technology that operates at 1V. The proposed circuit has simple symmetric structure and provides more stable operation while reducing spurious jump phenomenon. The output voltage of presented design can be increased up to 1015mV. The functionality of charge pump has been tested at operating based frequency of 400 MHz.

Keywords: Phase frequency detector (PFD), loop filter, voltage controlled oscillator (VCO), phase-locked loops (PLLs).

INTRODUCTION

The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, parallel and serial data communication, and frequency synthesizers. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the MHz frequency range. Hence there is a necessity of a mixed signal PLL which must operate in the MHz range with less lock time. The PLL performance depends upon its order. If 'n' is the order of loop filter than 'n+1' is the order PLL. The stability of the whole PLL system depends on the order of the loop filter. The voltage controlled oscillator (VCO) is the heart of the PLL. The present work focuses on the redesign of a PLL system using the 50nm technology. Hence a current starvedring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tunable frequency range. The Loop Filter described in this paper has been considered for its fast acquisition capability.

Phase locked loop is a feedback system that compares and locks the phase and frequency of an input signal withrespect to the available reference signal. The comparison is generally performed by a phase and frequency comparator which is technically known as phase frequency detector (PFD). The output of the PFD is fed to a charge pump circuit to get a constant current at the output. The charge pump output is passed through a low pass filter to generate the control voltage for the VCO circuit. Hence there are five functional blocks in a PLL circuit such as phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and frequency divider. The frequency divider is an optional block. It may or may not be included in the circuit diagram. The PLL architecture having all the above building blocks including the buffer is shown in the Fig.1. The details of all the blocks are explained in the following sections.

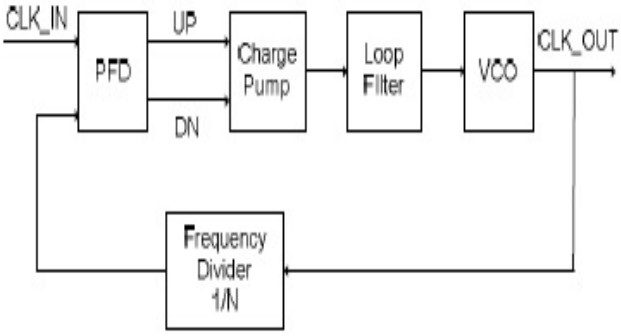

Figure 1: Phase Locked Loop

PHASE FREQUENCY DETECTOR

The PFD circuit is used to find the difference in phase and frequency between the two input signals reference frequency

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(Fref) and input frequency (Fin) which is fed back from the output of the VCO. The PFD generates two output signals UP and DOWN that switches the output current of the pump.PFDcircuit is generally implemented using D flip flops (DFFs) .The output of the PFD depends upon both phase and frequency of the input signals. Initially both the signals will be low. When one of the PFD input rises the corresponding output becomes high. The simulation waveforms of PFD when Fref leads Fin are shown in the Fig.2.

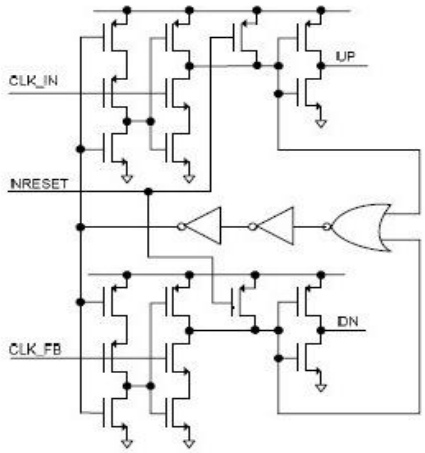

Figure 2: Phase and Frequency Detector

VOLTAGE CONTROLLED OSCILLATOR

The popular current starved ring oscillator is used as VCO in this study. Here the number of inverter stages is fixed with five. The schematic of the VCO is shown in the Fig.3.The center frequency of the VCO is 400MHz at 1 V supply. The inverter stages are designed as mentioned in [3], [5].Frequency depends on input voltage:

$$f=1/2RCln\,(1+Vcc/V)$$

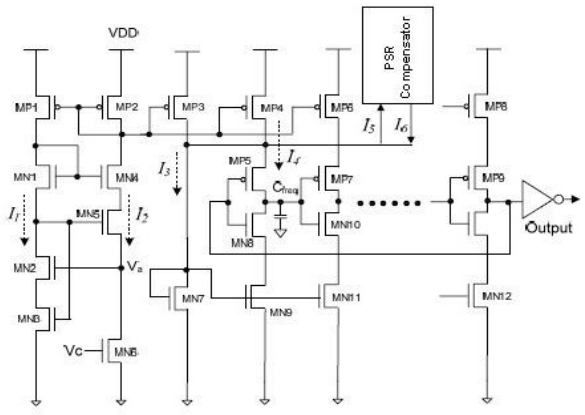

Figure 3: VCO

CHARGE PUMP

Charge pump circuit is used to combine both the outputsof the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value IPDI. The amplitude of the current always remains same but the polarity changes which depend on the value of the UPand DOWN signal. The schematic diagram of the charge pump circuit is shown in the Fig.4.When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is IPDI with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is IPDI with a negative polarity.

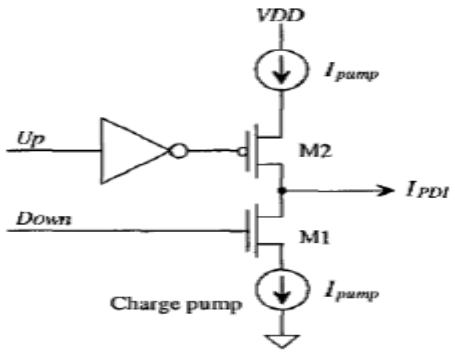

Figure 4: Simple Charge Pump

The charge pump output current is given by

$$I_{PDI} = K_{PDI} \times \Delta\varphi \qquad (1)$$

$$\text{Where } K_{PDI} = \frac{I_{PUMP}}{2\pi} \text{ (amps/radian)} \qquad (2)$$

$$\Delta\varphi = \varphi_{in} - \varphi_{ref} \qquad (3)$$

The phase difference Δφ is zero when loop is lock.The VCO input voltage is given by

$$V_{invco} = K_f \times I_{PDI} \qquad (4)$$

The passive low pass loop filter is used to convert back thecharge pump current into the voltage. The output voltage ofthe loop filter controls the oscillation frequency of the VCO.The loop filter voltage will increase if Fref leads Fin and will decrease if Fin leads Fref. If the PLL is in locked state it maintains a constant value.

Limitations of Simple PLL Architecture: For type I PLL there is always trade-offs between damping ratio of loop filter, loop filter bandwidth and the phase error. Hence the performance of PLL cannot improve beyond certain limit. Apart from this, a simple PLL suffers from a critical drawback i.e. limited acquisition range, Suppose when a PLL circuit is turned on, its oscillator operates at a frequency far from the input frequency, i.e. the loop is not locked. Now PLL starts acquiring a lock. The transition of

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the loop from unlocked to locked condition is very nonlinear process because phase detector senses unequal frequency. Also for this kind of PLL, the "acquisition range" is on order of ω_{LPF}, that is, the loop locks only if the difference between ω_{in} and ω_{out} is less than roughly ω_{LPF}. If ω_{LPF} is reduces to suppress the ripple on control voltage, the acquisition range decreases. Even if the input frequency has a precisely controlled value, a wide acquisition range is often necessary because the VCO frequency may vary considerably with the process and temperature. Hence in order to remove this problem, frequency detection is also incorporated in addition to phase detection. The concept is such that let the two frequencies (reference and VCO output frequency) be equal, once these two frequencies are equal, phases are compared and VCO is tuned such that phases of reference and feedback waveform are equal. Frequencies are analyzed in the s-domain. But the s-domain analysis is based on a continuous time approximation of the CPPLL and cannot accurately estimate the locking time. Besides s-domain analysis, two analyses using an event-driven non-linear model for a 2nd-order CPPLL in and state- space equations for a 3rd-order CPPLL in are proposed, which can provide exact models of the PLL dynamics. But it is difficult to set up or adapt these equations to other architectures especially for higher-order PLLs. In contrast behavioral models can be set up and modified for other applications or higher-order PLLs rather easily relative to provide a more accurate estimation of the locking time than s-domain analysis.

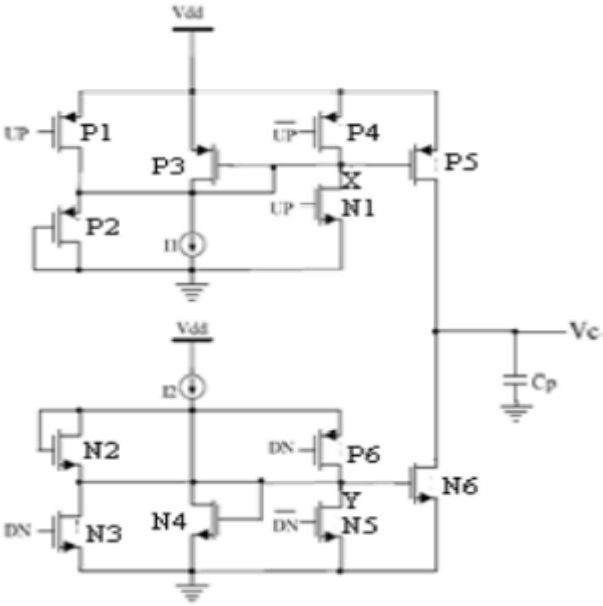

Figure 5: Improved Charge Pump

Improved Charge PUMP Structure: There are number of charge pump circuits were designed to reduce jump phenomenon from time to time. The proposed circuit, as shown in Fig.5, is a new way to achieve this purpose and increases the output voltage range. The Proposed charge pump circuit consists of pull-up & pull-down network. The charge pump circuit works as follows, When the signal UP =1 (high logical level), P1 is 'OFF' and the current source I1 drives P3. Since the power supply is 1V, when P3 is 'ON', the voltage enough to open it. Obviously, P5 is 'ON' and so P3 and P5 compose a current mirror. Capacitor Cp will be charged by the current source I1, raising the voltage Vc. In other hand DN =0 (Low logical level), pull down network is OFF. When the signal UP =0 (low logical level), P1 and P2 are both 'ON'. Since IP1=IP2+I1, The current in P3 and P5 are so small that they are negligible. Then, the voltage Vc at the capacitor should, ideally, remain stable.

P4 and N1 are used to predischarge to the gate of P5 (pre-discharge at the gate of N6). If they are cancelled in this charge pump circuit, when the UP signal is switched from 0 to 1, the charging time of P3 is relatively long, which results in delaying open speed of P5. So to overcome this problem, P4 and N1 are taken advantage at the gate of P5. Then, the voltage at the gate of P5 is rapidly pulled down once the UP signal switches from 0 to 1 opening P5 in a much shorter time. In other hand DN =1 (High logical level), pull-down network is 'ON' and capacitor Cp will be discharged. When they are both ON, they operate in the saturation region. So, to carry the same currents, P4 and N1 have to be perfectly matched (I 4=I 1). Meanwhile, in order to minimize the introduction of the parasitic capacitance, the width and length values of P4, N1 must be as small as possible.

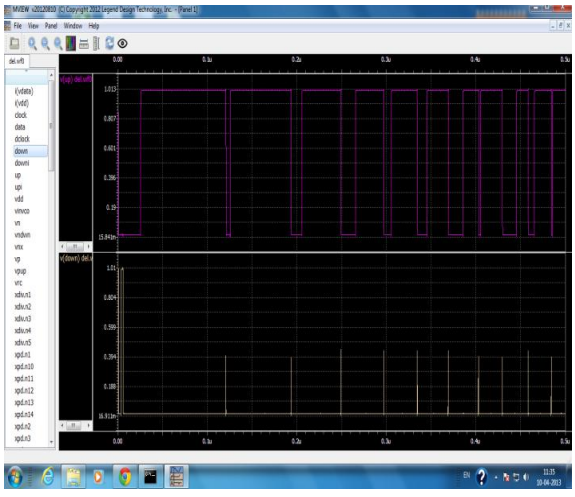

Figure 6: Up Voltage and Down Voltage

Simulations Results: The new charge pump circuit is designed in 50nm CMOS process, simulated using MSIM under a 1V power supply. The pull up current I1 and the pull

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down current I2 are both set to 10µA. The operating frequency is 400MHz and Fig. 6 shows the charging and discharging result of the new charge pump circuit. The output voltage range is from 995mV up to 1015mV.

A summary of the circuit characteristics is presented in Table I.

PARAMETER	RESULT
Power supply	1V
Operating Frequency	400 MHZ
Pull up and Pull down Current	10 µA
Output Voltage Range	995 mV to 1015 mV
Technology	50 nm CMOS

CONCLUSION

In this paper, a high speed CMOS charge pump for PLL application has been designed and simulated using the 50nm CMOS technology. The simple and symmetric structure of the circuit reduces spurious jitter phenomenon and provide more stable operation under a 1 V power supply without use of op-amp circuit. It has output voltage range from 995mV up to 1015mV and more stable step voltage. Simulations were done using MSIM. The pull-up current I1 and the pull down current I2 are both set to 10µA. The operating frequency is 400MHz.

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